**AXI Crossbar**

* Each instance of the AXI Interconnect core contains one AXI Crossbar instance (provided it is configured with more than one SI or more than one MI).
* The Slave Interface (SI) of the AXI Crossbar core can be configured to comprise 1-16 SI slots to accept transactions from up to 16 connected master devices. The Master Interface (MI) can be configured to comprise 1-16 MI slots to issue transactions to up to 16 connected slave devices.
* Selectable Interconnect Architecture
  + Crossbar mode (Performance optimized)
    - Shared-Address, Multiple-Data (SAMD) crossbar architecture.
    - Parallel crossbar pathways for Write data and Read data channels. When more than one Write or Read data source has data to send to different destinations, data transfers can occur independently and concurrently, provided AXI ordering rules are met.
    - Sparse crossbar datapaths according to configured connectivity map, resulting in reduced resource utilization.
    - One shared Write address arbiter, plus one shared Read address arbiter. Arbitration latencies typically do not impact data throughput when transactions average at least three data beats.
    - Crossbar mode is available only when AXI Crossbar is configured for AXI4 or AXI3 protocol.
  + Shared Access mode (Area optimized)
    - Shared write data, shared read data, and single-shared address pathways.
    - Issues one outstanding transaction at a time.
    - Minimizes resource utilization.
* Supports multiple outstanding transactions (crossbar mode)
  + Supports connected masters with multiple reordering depth (ID threads).
  + Supports up to 32-bit wide ID signals with varying ID width per connected master.
  + Supports write response re-ordering, Read data re-ordering, and Read Data interleaving.
  + Configurable Write and Read transaction acceptance limits for each connected master.
  + Configurable Write and Read transaction issuing limits for each connected slave.
  + Optional single-thread mode (per connected master) reduces thread control logic by allowing one or more outstanding transactions from only one thread ID at a time.
* “Single-Slave per ID” method of cyclic dependency (deadlock) avoidance

For each ID thread issued by a connected master, the Interconnect allows one or more outstanding transactions to only one slave device for Writes and one slave device for Reads, at a time.

* Fixed priority and round-robin arbitration
  + 16 configurable levels of static priority.
  + Round-robin arbitration is used among all connected masters configured with the lowest priority setting (priority 0), when no higher priority master is requesting.
  + Any SI slot that has reached its acceptance limit, or is targeting an MI slot that has reached its issuing limit, or is trying to access an MI slot in a manner that risks deadlock, is temporarily disqualified from arbitration, so that other SI slots can be granted arbitration.
* Supports TrustZone security for each connected slave as a whole
  + If configured as a secure slave device, only secure AXI accesses are permitted.
  + Any non-secure accesses are blocked and the AXI Interconnect core returns a decerr response to the connected master.